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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,204	02/25/2002	Kentaro Shimada	520.41277X00	2853

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EXAMINER	
CONTINO, PAUL F	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,204	SHIMADA, KENTARO	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 4 objected to because of the following informalities: use of comma at end of claim limitation. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 13 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "first n-th systems" where "n denotes 3 or larger." Language is indefinite, as interpretation of "n-th" could mean any system of three, e.g. n could equal zero through two, thereby causing confusion throughout the remainder of the claim. The metes and bounds of the claim cannot be determined. In order to apply prior art, the claim will be interpreted as n equaling at least three.

3. Claim 13 recites the limitation "the i-th output" in line 10. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 14 recites the limitation "said plurality of comparators" in line 14. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 11 rejected under 35 U.S.C. 102(b) as being anticipated by Carlson.

As in claim 11, Carlson discloses a first system and a second system having identical function to each other (Fig. 1 #102, 104, 106; column 2 lines 7-9, 26-45);

an input data buffer for temporarily storing input data to be supplied to said first and second systems (Fig. 1 # 120 (I), column 2 lines 46-48, column 3 lines 10-19);

a predecessor monitor for monitoring whether or not said first system has normally completed a processing operation on a unit of input data (Fig. 2 # 212, column 3 lines 42-43, column 4 lines 48-52);

and a successor controller for controlling start of processing operation by said second system on the input data already processed by said first system in accordance with a result of monitoring by said predecessor monitor (Fig.1 #118, column 3 lines 16-45).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-10, 12-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Carlson (U.S. Patent 5,892,897) in view of Klecka et al. (U.S. Patent 6,393,582).

As in claim 1, Carlson discloses a predecessor and a successor having identical function to each other (Fig. 1 #102, 104, 106; column 2 lines 7-9, 26-45);

an input data buffer for temporarily storing input data to be supplied to said predecessor and said successor (Fig. 1 # 120 (I); column 2 lines 46-48; column 3 lines 10-19);

an output data buffer for temporarily storing output data from said predecessor (Fig. 1 #112; column 3 lines 36-37);

a comparator for comparing output data from said successor with output data from said predecessor stored in said output data buffer (Fig. 1 #110; column 3 lines 36-38);

an execution controller for confirming that said predecessor has normally completed a processing operation on a unit of input data, allowing said successor to start an operation of processing input data which has been already processed by said predecessor (column 3 lines 2-33, 41-51).

However, Carlson does not teach of a gate for controlling outputting of said output data from said successor to the outside of the multiplex system in accordance with a result of the comparison by said comparator (Fig. 2 # 216; column 4 lines 48-56). Klecka et al. discloses a gate for controlling the results of a comparison (Fig. 1 #22; column 3 lines 9-12).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the "gate" as disclosed in Klecka et al. in the invention of Carlson. This would have been obvious because the use of a gate as disclosed in the system of Klecka et al. improves upon the similar functional system of Carlson by allowing for a more efficient and error-transparent fault recovery. Carlson discloses halting and scanning of processors in order to determine and recover from a fault, where Klecka et al. disclose an improvement to processor halting for fault recovery (column 1 lines 33-38 and column 2 lines 21-31) through implementation of an output device (column 2 line 5-9 where the output data transmission suspension is controlled by the I/O bridge "gate").

As in claim 2, Carlson and Klecka et al. disclose wherein said execution controller comprises:

a predecessor monitor for monitoring whether or not said predecessor has normally executed an operation of processing input data (Carlson: Fig. 2 # 212, column 3 lines 42-43,

column 4 lines 48-52; Klecka et al.: Fig. 1 #24 and 24a, column 3 lines 59-61, column 5 lines 54-64 where the ability of the master processor [predecessor] to assert an error signal to 24 [execution controller] combined with Carlson's disclosure of correct assumption of normal shadow [predecessor] processing would have been obvious to a person skilled in the art include in a single monitoring unit);

and a successor controller for controlling start of an operation of processing the next input data by said successor in accordance with a result of monitoring the operation of the predecessor by said predecessor monitor (Carlson: Fig.1 #118, column 3 lines 16-45; Klecka et al. Fig. 1 #24/30 which has ability to communicate data to shadow [successor] as previously stated in this office action).

As in claim 3, Klecka et al. discloses status recovering means for copying, when an operation failure of said predecessor is detected by said predecessor monitor, the status of said successor before start of processing on the input data to said predecessor, thereby recovering the status of said predecessor to the same status as that in said successor (column 1 lines 33-38, column 6 line 37 through column 7 line 46 where one skilled in the art would have found it obvious to have stored the original state of the master processor [predecessor] in memory 20 (column 7 lines 23-25) before processing of input data so that upon failure of master [predecessor] the loaded [copied] status (column 7 lines 40-45) from memory 20 would have contained the same status as in the shadow processor [successor] previous to the processing of the input data, since master and shadow processors were operating on the same data at the same time. Reasons for obviousness are discussed in Klecka et al. column 1 lines 33-38 where this

method is discouraged, but previously known to those skilled in the art, in order for a more efficient recovery. Regardless of whether recovery continues at point of failure or at start of original processing, the master processor [predecessor] ultimately operates on same data with same functionality at same points throughout processing; motivation, suggestion, or teaching from Carlson in column 1 lines 52-54 and column 4 lines 48-57).

As in claim 4, Klecka et al. discloses wherein said predecessor monitor has means for instructing said predecessor to re-process input data which has failed due to said operation failure at a predetermined timing after the status of said predecessor is recovered by said status recovering means (column 7 lines 32-36).

As in claim 5, Klecka et al. discloses wherein said execution controller has means for allowing, when discrepancy of output data of said predecessor and successor is detected by said comparator, said predecessor and successor to re-execute processing on input data corresponding to said output data (column 6 line 37 through column 7 line 46).

As in claim 6, Carlson and Klecka et al. disclose wherein said re-executing means confirms that said predecessor has normally finished the re-execution of processing on said input data and allows said successor to re-execute the processing on said input data (Carlson: Fig. 2 # 212, column 3 lines 42-43, column 4 lines 48-52; Klecka et al.: Fig. 1 #24 and 24a, column 3 lines 59-61, column 5 lines 54-64 [see claim 2]; inherent that the same confirmation and process would occur during re-execution as in original execution).

As in claim 7, Carlson and Klecka et al. disclose wherein said predecessor monitor includes output time-out detecting means for detecting whether or not a result is output within predetermined time since processing on a unit of input data is started (Carlson: column 3 lines 2-51 where the counter 118 in Fig. 1 is "time-out" with N-pipeline 112 as "monitor"; Klecka et al. column 4 lines 18-39 where timer is included in ICR 24 [predecessor monitor]).

As in claim 8, Klecka et al. discloses switching means for switching said successor controller from a normal mode to a reduced mode, when a failure occurs in reprocessing on the same input data by said predecessor, thereby to allow said successor controller to sequentially start the processing operation on next input data by said successor irrespective of a result of monitoring the operation of the predecessor by said predecessor monitor, and to deliver output data from said successor system to the outside via said gate (column 9 lines 33-45).

As in claim 9, Klecka et al. discloses wherein said switching means switches said successor controller to said reduced mode in response to a failure notification generated by said predecessor monitor when the number of repetitions of the reprocessing on the same input data by said predecessor becomes a predetermined number to carry out the switch. (column 9 lines 33-45, where the "number of repetitions" and "predetermined number" in Klecka et al. is interpreted as a single repetition and one, respectively).

As in claim 10, Klecka et al. discloses a successor monitor for monitoring whether or not said successor normally executes an operation of processing input data (Fig. 1 #24, column 3 lines 29-44);

and status recovering means for copying the status of said predecessor before start of processing on the next input data to said successor when an operation failure of said successor is detected by said successor monitor, thereby recovering the status of said successor to the same status as that in said predecessor (Fig. 3 and 5, column 7 line 59 through column 8 line 23).

* * *

As in claim 12, Carlson teaches the limitations of claim 11, but fails to teach the limitations of claim 12. Klecka et al. discloses means for copying, when an operation failure is detected in said first system by said predecessor monitor, a status of said second system to said first system and, at a predetermined timing, instructing said first system to re-process the input data which has not been successfully processed due to said operation failure (column 1 lines 33-38, column 6 line 37 through column 7 line 46 [see claim 3] and column 7 lines 32-36).

It would have been obvious for one skilled in the art at the time the invention was made to have included the means for copying as disclosed by Klecka et al. in the invention of Carlson. This would have been obvious because Klecka et al. discloses a means for copying and reprocessing which Carlson references as background in column 1 lines 52-54.

* * *

As in claims 13 and 15, claim 13 is interpreted as stating a system with at least three units – which is addressed in the scope of the three units of claim 15. Regardless of the number of units, no new novelty exists within the limitations stated in claim 13 when related to claim 15.

As in claim 15, Carlson discloses a first, second, and third system having identical function to each other (Fig. 1 # 120 (I); column 2 lines 46-48; column 3 lines 10-19).

an input data buffer for temporarily storing input data to be supplied to said first, second, and third systems (Fig. 1 # 120 (I); column 2 lines 46-48; column 3 lines 10-19).

a first output data buffer for temporarily storing output data from said first system (Fig. 1 #112; column 3 lines 36-37);

a first comparator for comparing the output data from said second system with the output data from said first system stored in said first output data buffer (Fig. 1 #110; column 3 lines 36-38);

a first execution controller for confirming that said first system has normally completed a processing operation on a unit of input data, and allowing said second system to start an operation of processing the input data already processed by said first system (column 3 lines 2-33, 41-51);

However, Carlson fails to teach of a gate, a second output data buffer, a second comparator, and a second execution controller. Klecka et al. teaches a gate for controlling delivering of said output data to the outside in accordance with results of the comparison by said comparators (Fig. 1 #22; column 3 lines 9-12);

It would have been obvious to a person skilled in the art at the time the invention was made to have included the "gate" as disclosed in Klecka et al. in the invention of Carlson. This

would have been obvious because the use of a gate as disclosed in the system of Klecka et al. improves upon the similar functional system of Carlson by allowing for a more efficient and error-transparent fault recovery. Carlson discloses halting and scanning of processors in order to determine and recover from a fault, where Klecka et al. disclose an improvement to processor halting for fault recovery (column 1 lines 33-38 and column 2 lines 21-31) through implementation of an output device (column 2 line 5-9 where the output data transmission suspension is controlled by the I/O bridge "gate").

It would have been obvious to a person skilled in the art at the time the invention was made to have configured the master, shadow, and trailer processors as disclosed in Carlson as a "first, second, and third system," respectively. This would have been obvious because one skilled in the art would have known that by replacing the known "good" and "bad" processors as disclosed in Carlson's system with "unknown" processors, results would have been consistent with applicant's claimed limitations within the scope of Carlson in view of Klecka et al.

It would also have been obvious to a person skilled in the art at the time the invention was made to have included a second output data buffer from said second system, a second comparator comparing said second and third systems, and a second execution controller between the second and third systems, as between the first and second systems, in order for proper functioning to receive the desired results in such a system, in view of previous paragraph. This would have been obvious because the number of components has changed to accommodate the number of processors, not the functionality or the configuration of the components. In order to accommodate a three processor system, one skilled in the art would have thought it obvious to have included duplicate components interfacing said three processors in a similar manner as said

two processor system in order to achieve proper and similar system confirmation as between said two processor system.

* * *

As in claim 14, Carlson disclose a first, second, and third systems having identical function to each other (Fig. 1 #102, 104, 106; column 2 lines 7-9, 26-45);

an input data buffer for temporarily storing input data to be supplied to said first, second, and third systems (Fig. 1 # 120 (I); column 2 lines 46-48; column 3 lines 10-19);

an output data buffer for temporarily storing output data from said first system (Fig. 1 #112; column 3 lines 36-37);

a comparator for comparing output data from said second system with output data from said first system, stored in said output data buffer (Fig. 1 #110; column 3 lines 36-38);

a first execution controller for confirming that said first system has normally completed a processing operation on a unit of input data, and allowing said second system to start an operation of processing the next input data already processed by said first system (column 3 lines 2-33, 41-51);

However, Carlson fails to teach a gate, a second execution controller, and a means for copying status of systems. Klecka et al teaches a gate for controlling delivering of said output data from said second system to the outside in accordance with results of the comparison by said comparator (Fig. 1 #22; column 3 lines 9-12), and

and means for copying a status of said third system to said first and second systems when discrepancy of output data is detected by said comparator (column 1 lines 33-38, column 6 line 37 through column 7 line 46 [see claim 3]).

It would have been obvious to a person skilled in the art at the time the invention was made to have included the gate as disclosed in Klecka et al. in the invention of Carlson. This would have been obvious because the use of a gate as disclosed in the system of Klecka et al. improves upon the similar functional system of Carlson by allowing for a more efficient and error-transparent fault recovery. Carlson discloses halting and scanning of processors in order to determine and recover from a fault, where Klecka et al. disclose an improvement to processor halting for fault recovery (column 1 lines 33-38 and column 2 lines 21-31) through implementation of an output device (column 2 line 5-9 where the output data transmission suspension is controlled by the I/O bridge "gate").

It would have been obvious for one skilled in the art at the time the invention was made to have included the means for copying as disclosed by Klecka et al. in the invention of Carlson. This would have been obvious because Klecka et al. discloses a means for copying and reprocessing which Carlson references as background in column 1 lines 52-54.

It would have been obvious to a person skilled in the art at the time the invention was made to have configured the master, shadow, and trailer processors as disclosed in Carlson as a "first, second, and third system," respectively. This would have been obvious because one skilled in the art would have known that by replacing the known "good" and "bad" processors as disclosed in Carlson's system with "unknown" processors, results would have been consistent with applicant's claimed limitations within the scope of Carlson in view of Klecka et al.

It would also have been obvious to a person skilled in the art at the time the invention was made to have included an identical second execution controller between the second and third systems, as between the first and second systems, in order for proper functioning to receive the desired results in such a system, in view of previous paragraph. This would have been obvious because the number of components has changed to accommodate the number of processors, not the functionality or the configuration of the controllers. In order to accommodate a third processor, one skilled in the art would have thought it obvious to have included a second controller between the second and third processors in order to achieve proper and similar system confirmation as between the first and second processors.

As in claim 16, Klecka et al. discloses wherein said first execution controller has means for copying, when an operation failure is detected in said first system, a status of said second system before a processing on next input data is started into said first system, and allowing the first system to re-execute processing on input data which has not been successfully processed due to said operation failure (column 1 lines 33-38, column 6 line 37 through column 7 line 46 [see claim 3] and column 7 lines 32-36), and

said second execution controller has means for copying, when an operation failure is detected in said second system, a status of said third system before processing on next input data is started into said second system, and allowing the second system to re-execute process on input data which has not been successfully processed due to said operation failure (column 1 lines 33-38, column 6 line 37 through column 7 line 46 [see claim 3] and column 7 lines 32-36; [see claim 14 obviousness statement]).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (703) 605-4316 [after approximately October 15, 2004 at (571) 272-3657]. The examiner can normally be reached on Monday-Friday 7:30 am - 5:00 pm, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713 [after approximately October 15, 2004 at (571) 272-3645]. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 [after approximately October 15, 2004 at (571) 273-3657].

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PFC
September 9, 2004

SCOTT BADERMAN
PRIMARY EXAMINER